



October 1995  
Revised June 2000

# NC7S02

## TinyLogic™ HS 2-Input NOR Gate

### General Description

The NC7S02 is a single 2-Input high performance CMOS NOR Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V<sub>CC</sub> range. ESD protection diodes inherently guard both inputs and output with respect to the V<sub>CC</sub> and GND rails. Three stages of gain between inputs and outputs assures high noise immunity and reduced sensitivity to input edge rate.

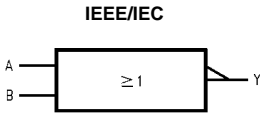
### Features

- Space saving SOT23 or SC70 5-lead packages
- High Speed; t<sub>PD</sub> 3.5 ns typ
- Low Quiescent Power; I<sub>CC</sub> < 1 μA
- Balanced Output Drive; 2 mA I<sub>OL</sub>, -2 mA I<sub>OH</sub>
- Broad V<sub>CC</sub> Operating Range; 2V-6V
- Balanced Propagation Delays
- Specified for 3V operation

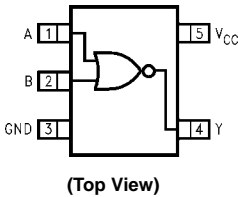
### Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7S02M5	MA05B	7S02	5-Lead SOT23, JEDEC MO-178, 1.6mm	250 Units on Tape and Reel
NC7S02M5X	MA05B	7S02	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7S02P5	MAA05A	S02	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	250 Units on Tape and Reel
NC7S02P5X	MAA05A	S02	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
A, B	Inputs
Y	Output

### Function Table

$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level  
L = LOW Logic Level

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**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
@ $V_{IN} \leq -0.5V$	-20 mA
@ $V_{IN} \geq V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
@ $V_{OUT} < -0.5V$	-20 mA
@ $V_{OUT} > V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_{OUT}$ )	$\pm 12.5$ mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 25$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	150°C
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C
Power Dissipation ( $P_D$ ) @ +85°C	
SOT23-5	200 mW
SC70-5	150 mW

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to 6.0V
Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC}$ @ 2.0V	0 to 1000 ns
$V_{CC}$ @ 3.0V	0 to 750 ns
$V_{CC}$ @ 4.5V	0 to 500 ns
$V_{CC}$ @ 6.0V	0 to 400 ns
Thermal Resistance ( $\theta_{JA}$ )	
SOT23-5	300°C/W
SC70-5	425°C/W

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specifications.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

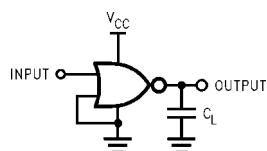
Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	2.0 3.0-6.0	1.50 0.7 $V_{CC}$			1.50 0.7 $V_{CC}$		V	
$V_{IL}$	LOW Level Input Voltage	2.0 3.0-6.0			0.50 0.3 $V_{CC}$		0.50 0.3 $V_{CC}$	V	
$V_{OH}$	HIGH Level Output Voltage	2.0	1.90	2.0		1.90		V	$I_{OH} = -20 \mu\text{A}$ $V_{IN} = V_{IL}$
		3.0	2.90	3.0		2.90			
		4.5	4.40	4.5		4.40			
		6.0	5.90	6.0		5.90			
		3.0	2.68	2.85		2.63		V	$V_{IN} = V_{IL}$ $I_{OH} = -1.3 \text{ mA}$ $I_{OH} = -2 \text{ mA}$ $I_{OH} = -2.6 \text{ mA}$
		4.5	4.18	4.35		4.13			
		6.0	5.68	5.85		5.63			
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.10		0.10	V	$I_{OL} = 20 \mu\text{A}$ $V_{IN} = V_{IH}$
		3.0		0.0	0.10		0.10		
		4.5		0.0	0.10		0.10		
		6.0		0.0	0.10		0.10		
		3.0		0.1	0.26		0.33	V	$V_{IN} = V_{IH}$ $I_{OL} = 1.3 \text{ mA}$ $I_{OL} = 2 \text{ mA}$ $I_{OL} = 2.6 \text{ mA}$
		4.5		0.1	0.26		0.33		
		6.0		0.1	0.26		0.33		
$I_{IN}$	Input Leakage Current	6.0			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = V_{CC}, \text{ GND}$
$I_{CC}$	Quiescent Supply Current	6.0			1.0		10.0	$\mu\text{A}$	$V_{IN} = V_{CC}, \text{ GND}$

# AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	5.0		3.5	15			ns	C <sub>L</sub> = 15 pF	Figures 1, 3
		2.0		19	100		125			
		3.0		10.5	27		35	ns	C <sub>L</sub> = 50 pF	
		4.5		7.5	20		25			
		6.0		6.5	17		21			
t <sub>TLH</sub> , t <sub>THL</sub>	Output Transition Time	5.0		3	10			ns	C <sub>L</sub> = 15 pF	Figures 1, 3
		2.0		25	125		155			
		3.0		16	35		45	ns	C <sub>L</sub> = 50 pF	
		4.5		11	25		31			
		6.0		9	21		26			
C <sub>IN</sub>	Input Capacitance	Open		2	10		10	pF		
C <sub>PD</sub>	Power Dissipation Capacitance	5.0		6				pF	(Note 3)	Figure 2

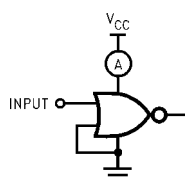
**Note 3:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2.) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:  
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$ .

## AC Loading and Waveforms



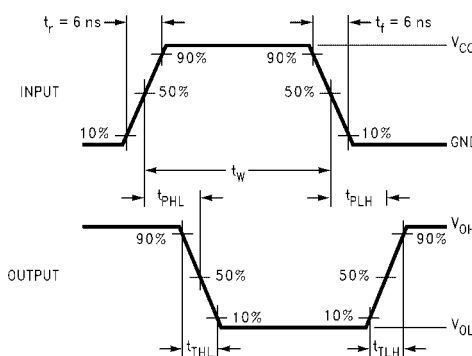
C<sub>L</sub> includes load and stray capacitance  
 Input PRR = 1.0 MHz; t<sub>w</sub> = 500 ns

**FIGURE 1. AC Test Circuit**



Input = AC Waveform;  
 PRR = variable; Duty Cycle = 50%

**FIGURE 2. I<sub>CCD</sub> Test Circuit**



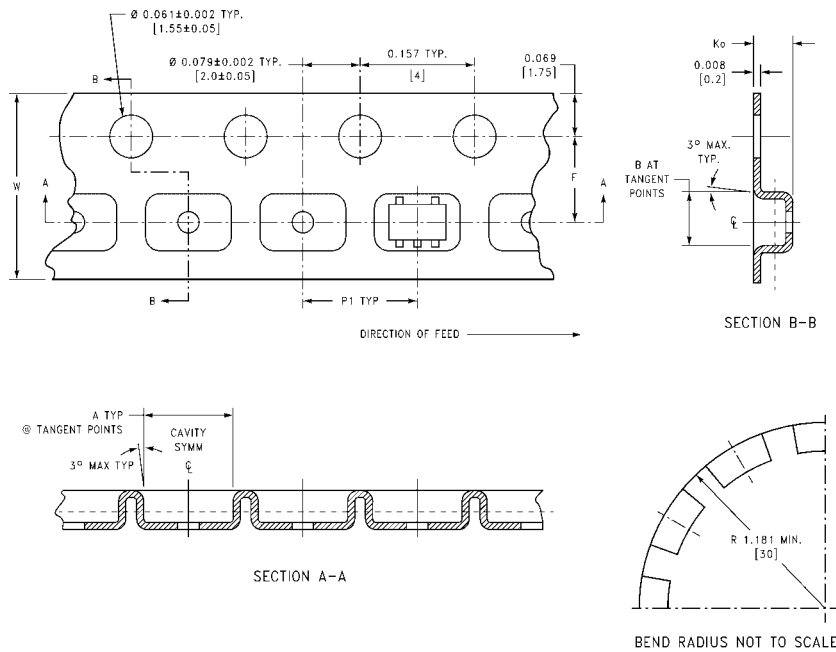
**FIGURE 3. AC Waveforms**

## Tape and Reel Specification

### TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5, P5	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

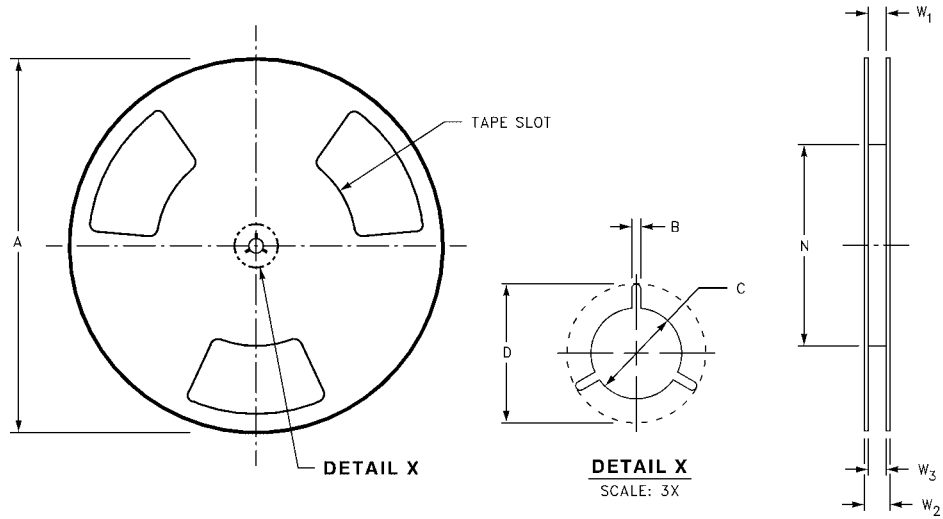
### TAPE DIMENSIONS inches (millimeters)



Package	Tape Size	DIM A	DIM B	DIM F	DIM $K_0$	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	$0.138 \pm 0.004$ ( $3.5 \pm 0.10$ )	$0.053 \pm 0.004$ ( $1.35 \pm 0.10$ )	0.157 (4)	$0.315 \pm 0.004$ ( $8 \pm 0.1$ )
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	$0.138 \pm 0.002$ ( $3.5 \pm 0.05$ )	$0.055 \pm 0.004$ ( $1.4 \pm 0.11$ )	0.157 (4)	$0.315 \pm 0.012$ ( $8 \pm 0.3$ )

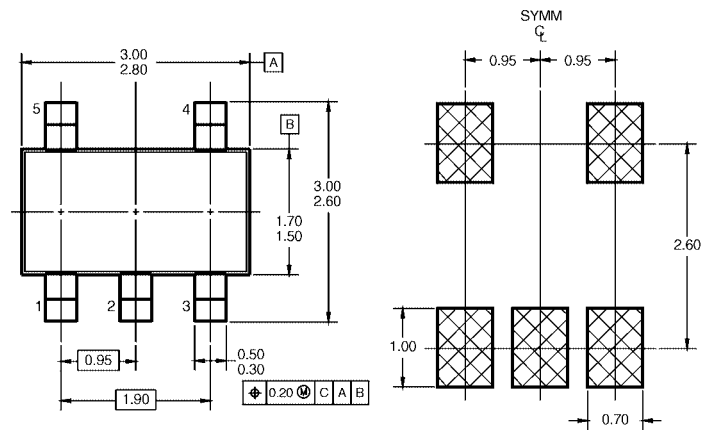
# Tape and Reel Specification (Continued)

REEL DIMENSIONS inches (millimeters)

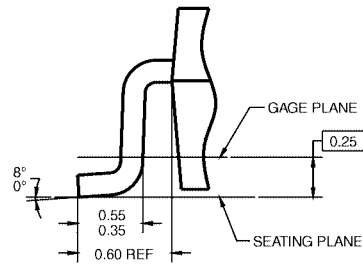
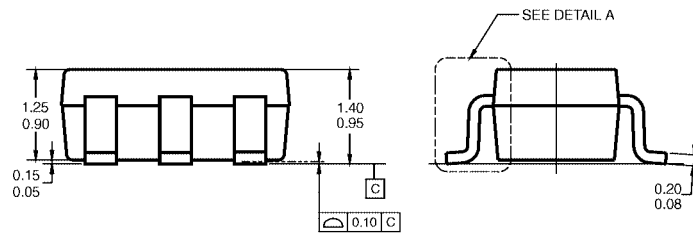


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

# Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



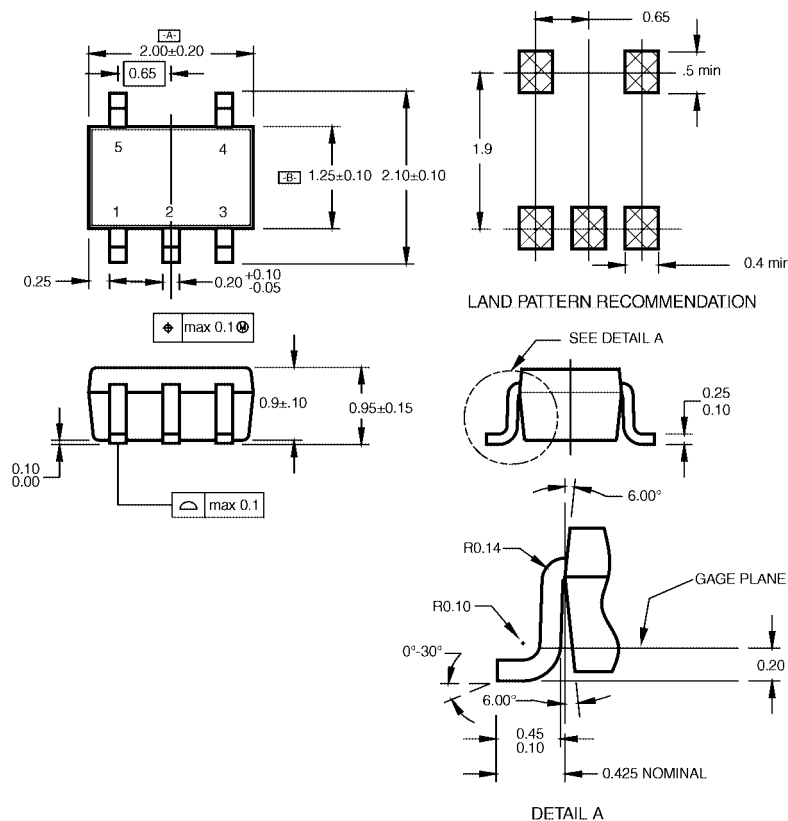
DETAIL A

- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

**5-Lead SOT23, JEDEC MO-178, 1.6mm  
 Package Number MA05B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**NOTES:**

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide  
Package Number MAA05A**

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